ISSN impreso 1996-6660 / ISSN online 2519-5719
DOI: https://doi.org/10.31381/perfilesingenieria.v20i21.5967

Low transconductance OTAs design with extended linear range and its application in EEG signals

Diseño de OTAs de baja transconductancia con rango lineal extendido y sus aplicaciones en señales EEG

Franco Renato Campana Valderrama

RECIBIDO: 10 de enero de 2024.
ACEPTADO: 27 de marzo de 2024.

Resumen

En este trabajo se presenta el diseño de OTAs simétricos con bajo valor de Transconductancia (orden de los nA/V) y sus aplicaciones en baja frecuencia y baja potencia. Para este objetivo, se usó espejos de corriente serie-paralelo (S-P), los cuales dividen la transconductancia del par diferencial. Con esta técnica se obtuvo transconductores de hasta 1 nA/V. También se presenta una técnica para extender el rango lineal de los pares diferenciales. Los OTAs simétricos diseñados serán usados en filtros activos de baja frecuencia central para aplicaciones biomédicas (señales EEG). Los capacitores de estos filtros están en el orden de los picofaradios y están fuera del circuito integrado. Estos OTAs y Filtros fueron diseñados con tecnología estándar de fabricación de 0.8 um. La factibilidad de las técnicas que presentaremos, serán validadas mediante resultados de simulación.

Palabras clave: amplificador, baja transconductancia, microconsumo, baja frecuencia, espejos de corriente.

Abstract

In this work, the design of symmetric OTAs with low transconductance value (nA/V order) and their application in low frequency and low power is presented. For this aim, the series-parallel (S-P) mirrors was used, which divided the differential pair transconductance. With this technique, a 1 nA/V transconductor is reached. Techniques for extend the linear range (hundreds milivolts) of the differential pair will presented too. The Advanced Compact MOSFET Model ACM was used in the design process. These symmetric OTAs designed will be used in active filters with low central frequency, for biomedical applications (EEG signals). The capacitors of this filters are in the picofaradads order, and are off chip. These OTAs and filters were designed in 0.8 um standard technology. These techniques that we will present will be validated through simulation

Keywords: amplifier, low transconductance, low power, low frequency, current mirrors.

Cómo citar

F. R. Campana Valderrama, «Low Transconductance OTAs Design with Extended Linear Range and its Application in EEG Signals», Perfiles_Ingenieria, vol. 20, n.º 21, pp. 151-164, jun. 2024.

1. Introduction

In the field of medical electronics, active filters with very low cutoff frequencies (of the order of a few hertz) are needed due to the relatively slow electrical activity of the human body. Specific applications ECG, EEG systems and pacemakers [1].

For an operational transconductance amplifier-capacitor (OTA-C) filter implementation, such low frequencies imply large capacitors and very low transconductances. Thus, there are two entirely independent angles to the problem that need to be addressed. One is the design of OTAs with very low transconductances (typically of the order of a few nanoamperes per volt) and high linearity, while the other is the realization of very large capacitors (typically of the order of a few nanofarads) on chip [1].

In this work shows by post layout simulations the feasibility of the OTAs design with low value of transconductance G_m and its application in active filters with low central frequency. For the OTAs designed, the main characteristics to be considered are: extended linear range at input (above 100 mV), low power consumption and low G_m value.

The ACM equations that will be used in the differential pair design will be presented in section 2. In section 3 will described the methodology design for OTAs with low G_m values, using the series-parallel S-P current division technique, which will allow us to divide the differential pair input transconductance. This paper presents the improvements in terms of current consumption, input linear range and area, from that achieved in reference [2].

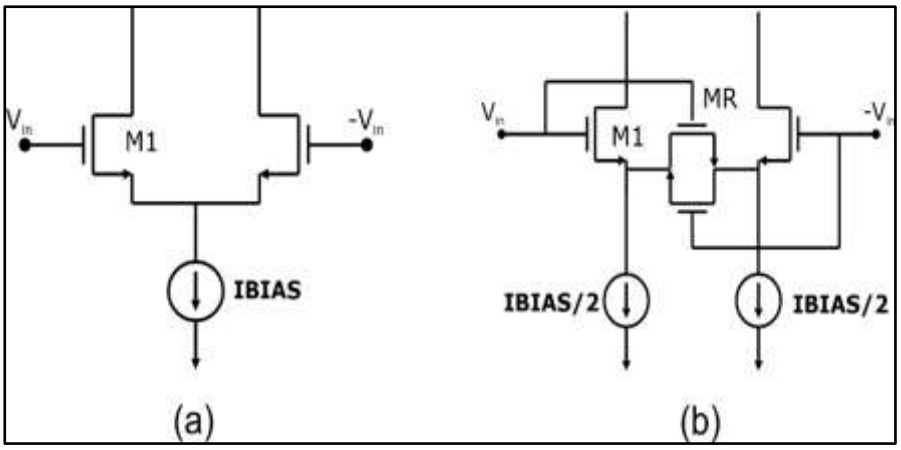
In section 4, it details the use of these OTAs in active Bandpass Filters with low central frequency, and will be used in the brain waves filtering (EEG signals). Finally, in section 5 will give some conclusions.

2. Differential Pair Design

The ACM Mosfet model will be used to calculate the differential pair linear range in tems of level inversion i_f . From figure 1(a):

ISSN (Digital): 2519-5719

Figure 1(a).
(a) Differential MOS pair, and (b) Differential MOS pair with active linearization



The relevant equations that will be useful to design from the input pair linearity in terms of level inversion are [3]:

$$V_{lin} \approx 3n\phi_t\sqrt{\alpha\left(1+i_f\right)} \quad (1)$$

The equation (1) is very useful in the theoretical design stage of any differential pair circuit. This expression will be valid in all levels inversion. The α value can be 0.05 or 0.1, and represent the expected percentage error \cite{arnaud1}. The i_f values can be $1<i_f$ for weak inversion, $i_f>100$ for strong inversion and $1<i_f<100$ for moderate inversion. For more details about the ACM model and their relationships in levels inversion terms, could be found in the [4] reference.

To enhance the linearity, a modified differential input pair can substitute M1 and M2 in Fig. 1(a), as shown in Fig.1(b) [5] . The effective transconductance g_{meff} of the pair in Fig. 1(b) is calculated by small signal analysis, assuming that transistors MR operate in the linear region, each behaving as a resistor of value 2R. Therefore:

$$g_{meff} = \frac{g_{m1}}{1+ng_{m1}R} \quad (2)$$

where g_{m1} is the trasnconductance pair, R is the degeneration resistor that can made with MOS transistor (M_R in Fig. 1(b)) and n is the slope factor, slightly greater than unity and weakly dependent on the gate voltage [6].

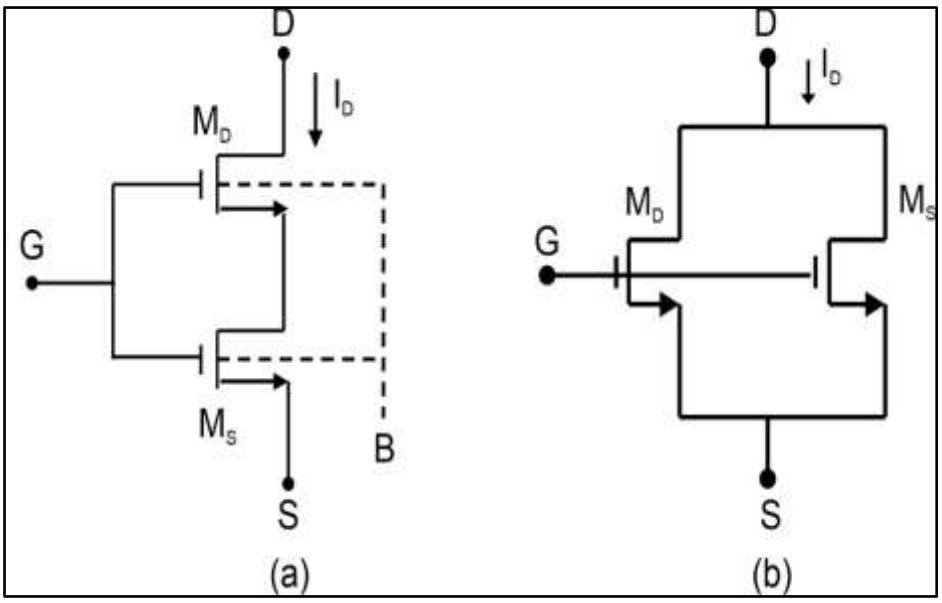
3. Ota Design Methodology

Here we examine the use of the series-parallel S-P technique, in order to apply in the symmetric OTAs circuit; with this technique could be divide the input pair transconductance for hundreds and allows the implementation of an area efficient current divider [6].

In Fig. 2(a) two transistors MS(D), are series connected; the equivalent ratio $(W/L)_{eq}$ of the composite transistor is [7]:

$$(W/L)_{eq} = \frac{(W/L)_S(W/L)_D}{(W/L)_D+(W/L)_S} \quad (3)$$

Figure 2.
(a) Two series transistors associated and (b) Two parallel transistors associated



From this equation, if the M_S and M_D transistors have the same (W/L), result will be (W/2L), it means that with the same aspect ratio (W/L) for transistors connected as in Fig. (2), the equivalent transistor aspect ratio it will be divided by 2. If it is generalized to "N" transistors in series with the same aspect ratio, the result will be (W/NL), namely, the equivalent transistor aspect ratio it will be divided by N.

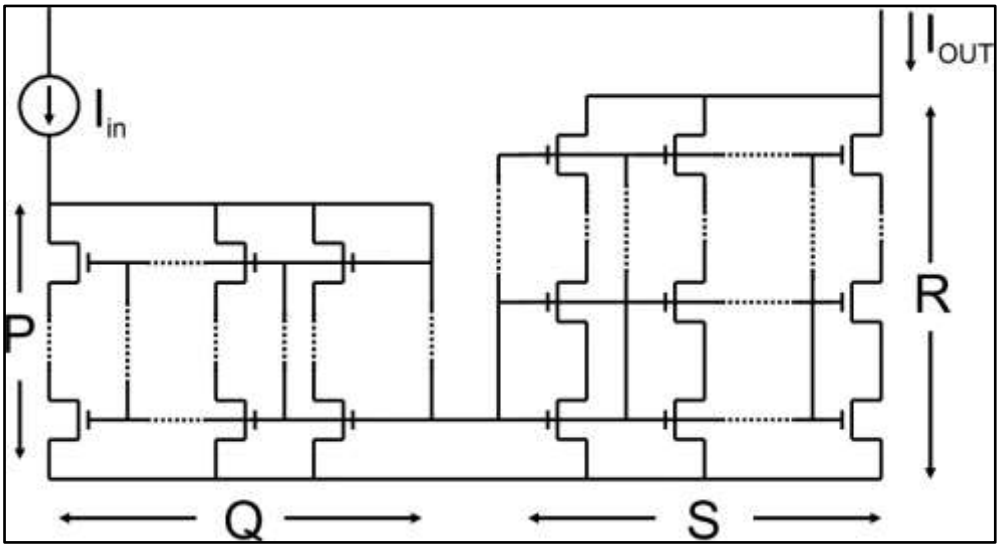
In the same way, if it has two transistors associated in parallel as in Fig. 2(b), the equivalent relationship $(W/L)_{eq}$ will be:

$$(W/L)_{eq} = (W/L)_D + (W/L)_S \quad (4)$$

For the last equation, if the transistors have the same aspect ratio (W/L), the result aspect ratio will be (2W/L). If it is generalized to "N" transistors in parallel with the same aspect ratio, the result will be (MW/L). This analysis can be extended up to achieve the topology shows in Fig. (3), that represents the S-P technique, applied to a simple current mirror [6]

ISSN (Digital): 2519-5719

Figure 3.
Generic SP current mirror



where:

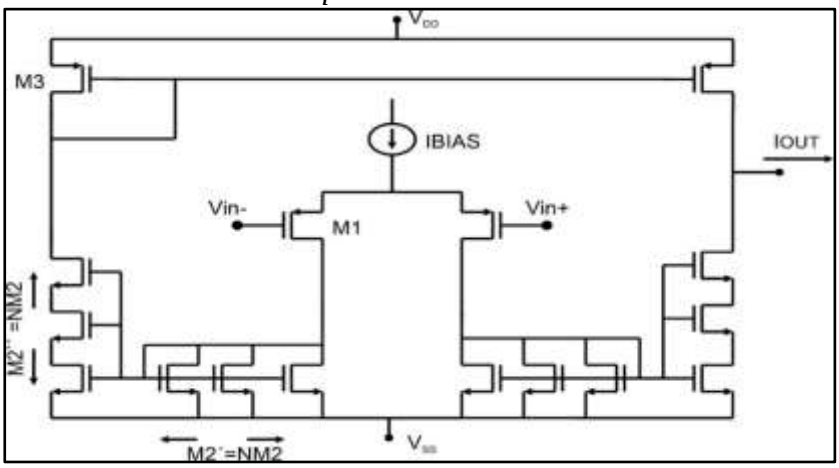
$$\frac{I_{OUT}}{I_{IN}} = \frac{SP}{RQ} \quad (5)$$

If in the last relationship we do S=P=1 with R=Q=N, we obtain:

$$\frac{I_{OUT}}{I_{IN}} = \frac{1}{N^2} \quad (6)$$

Applying the last equation to a symmetric OTA, we get the following circuit:

Figure 4.
Symmetric OTA with S-P technique



For the mirrors of Fig. (4), N transistors are associated in series an parallel to achieve the output transconductance [2], [3], [6]:

$$G_{mx} = g_{m1}\frac{SP}{RQ} = \frac{g_{m1}}{N^2} \quad (7)$$

where, g_{m1} is the differential pair transconductance, given by:

$$g_m = \frac{2I_D}{n\phi_t(\sqrt{1+i_f}+1)} \quad (8)$$

where ϕ_t is the thermodynamic voltage, and its 26 mV at room temperature.

Now, we show the strategy to follow to get OTAs with low transconductance and extended input linear range. The relationship between linear range input pair and level inversion i_f is given by the eq. (1).

Suppose that the circuit of the Fig. (4) requires a transconductor of a low value G_{mx}, and an input linear range V_{linx} with an α give by 5%. The inversion level i_{f1} of the input pair is determined by eq. (1). For a given bias current, that can be determined from the power consumption and area budgets, we have $I_{BIAS}=2I_{D1}$, and according to the ACM model, we have $I_{D1}=I_{SQ}(W/L)_1 i\_{f1}$, where I_{SQ} depends of the technology, therefore the $(W/L)_1=I_{BIAS}/(2I_{SQ}i_{f1})$. So, with the with the I_{BIAS}, α and i_{f1} give by eq. 1 according to linear range requirements, we can get the $(W/L)_1$ and g_{m1} by eq. 8. With this g_{m1}, could be obtain the number of unit transistors "N" or any arrangement unit transistor given by Eq. 7 [3].

With this technique it designed four OTAs with different transconductance input values. For example, with i_f=40, according to Eq. 1, we obtain V_{lin}=150mV, and with I_{BIAS}=80 nA, the G_{m1}=297nA/V. In the table 1 we detail these circuits.

Table 1.
Summary of Transistors Arrangement

OTA	G_{mx}	M_1	Arr	$(W/L)_u$	M_2'	M_2''	M_3	$(W/L)_u$
1	4.4 nS	(3/50)	5s	(3/10)	17p	8s x 2p	2s x 4p	(4/4)
2	8.8 nS	(3/50)	5s	(3/10)	17p	6s x 3p	2s x 4p	(4/4)
3	1.2 nS	(3/50)	5s	(3/10)	31p	16s x 2p	2s x 4p	(4/4)
4	15.6 nS	(3/50)	5s	(3/10)	8p	5s x 2p	2s x 4p	(4/4)

As an example, we can extend the input linear range based in the circuit of Fig.1(b), for all these OTAs and using the Eq.2. The G_{mx} target, M_1 and M_3 aspect ratio and its unitary arrangement are the same as table 1, so we do not repeat here. The table 2 present the aspect ratios resume.

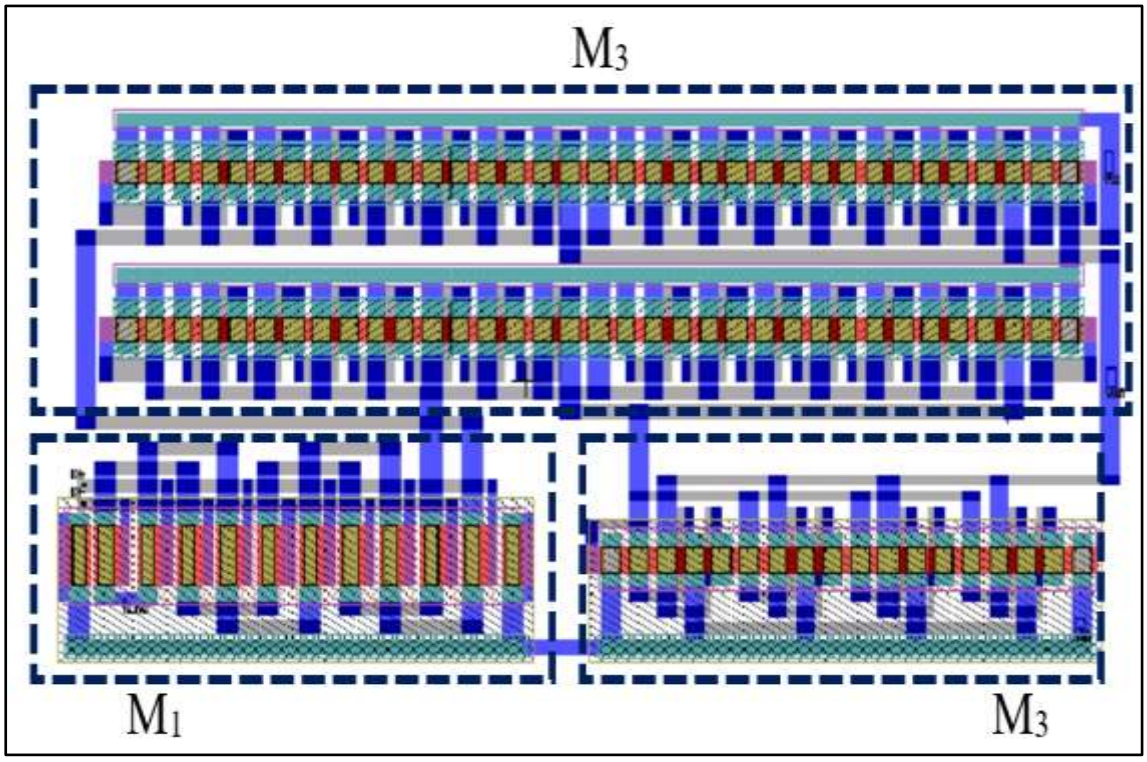
ISSN (Digital): 2519-5719

Table 2.
Transistors Arrangement for Extended Linear Range

OTA	$(W/L)_R$	M_2'	M_2''	$(W/L)_u$
1	(3/250)	10p	6s x 2p	(4/4)
2	(3/250)	15p	4s x 4p	(4/4)
3	(3/250)	12p	9s	(4/4)
4	(3/250)	6p	3s x 2p	(4/4)

As an example of layout, we show the layout of OTA 1 in Fig. (5). The layout technique used for all these circuits was the common centroid.

Figure 5.
Layout of OTA 1 of Table I



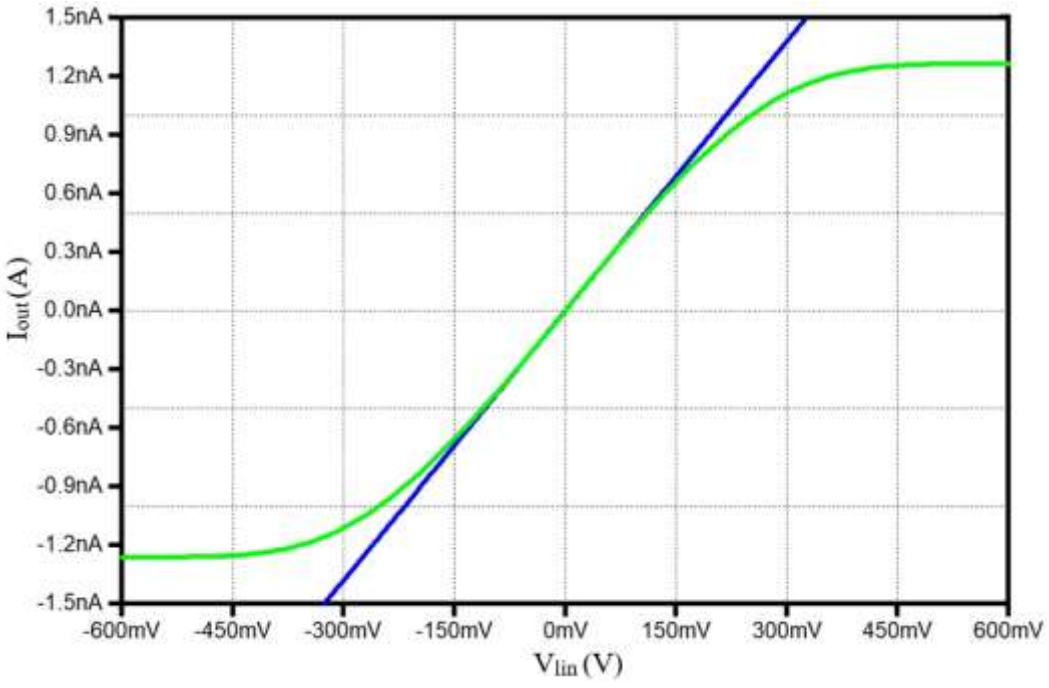
Here, we show in the table 2, a comparative survey using these technique and the requirements achieve, with the other topologies and techniques used for the requirements listed above.

Table 3.
Comparative Table off this Work with other Circuits

Parameters	OTA	SD+CD	FG+CD	BD+CD	This Work	
G_m (nS)	11.6	11.55	11.5	11.24	4.4	8.8
					1.2	15.6
Linearity (mVp)	80	120	165	450	150-500	150-500
					150-500	150-500
I_{BIAS} (nA)	2	100	200	500	80	80
					80	80
Power	16.2 nW	1.35 uW	1.62 uW	4.05 uW	406-417 nW	413-429 nW
					402-404 nW	422-450 nW
Area (mm^2)	1.44	0.21	4.65	0.22	0.023	0.026
					0.042	0.028

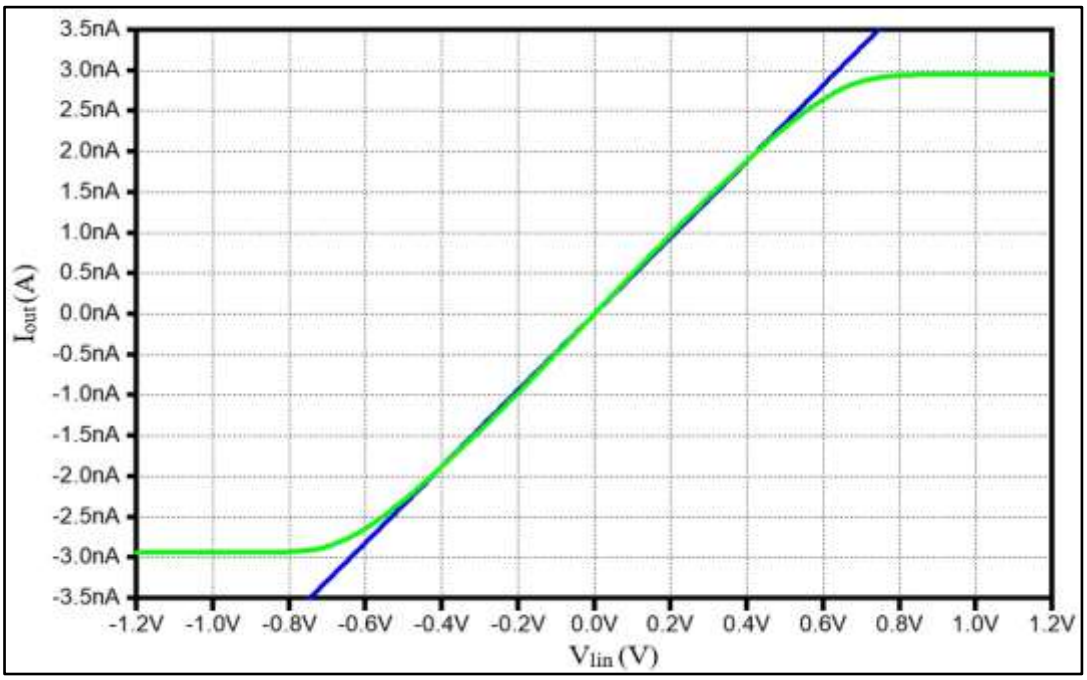
Where, according to [1]: OTA: Symmetric OTA, SD: Source degeneration, FG: Floating gate, BD: Bulk driven, CD: Current division. As an example, in the figure 6 and 7, we show the input linear range I_{out} vs. V_{lin} and extended linear range achieved in this work for OTA 1.

Figure 6.
Transfer curve I_{OUT} vs. V_{lin} of OTA 1



ISSN (Digital): 2519-5719

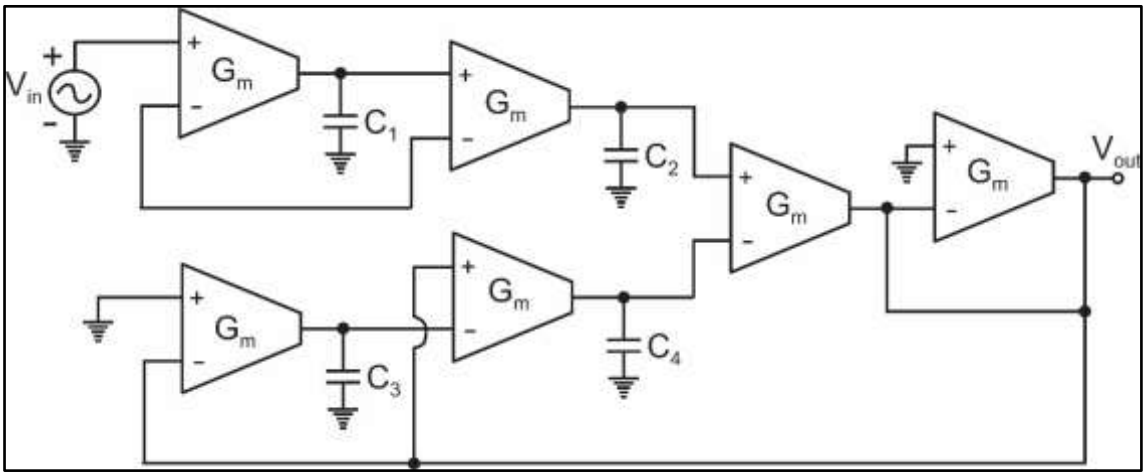
Figure 7.
Transfer curve IOUT vs. Vlin for extended linear range OTA 1



4. Filter Design

In the Fig. (8) we show the biquad filter structure [8] that we use to achieve a low centra frequencies.

Figure 8.
Bandpass filter topology



and the function transfer function is:

$$H(S) = \left[\frac{W_{P1}^2}{S^2+S(W_{P1}/Q_{P1})+W_{P1}^2}\right]\left[\frac{S^2}{S^2+S(W_{P2}/Q_{P2})+W_{P2}^2}\right] \quad (9)$$

and the equations project design will be:

$$C_1 = \frac{G_{m1}}{Q_{P1}W_{p1}}, C_2 = \frac{G_{m2}Q_{P1}}{W_{p1}}, C_3 = \frac{G_{m3}}{Q_{P2}W_{p2}}, C_4 = \frac{G_{m4}Q_{P2}}{W_{p2}} \quad (10)$$

$$W_{p1} = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}}, W_{p2} = \sqrt{\frac{G_{m3}G_{m4}}{C_3C_4}}, Q_{p1} = \sqrt{\frac{C_2G_{m1}}{C_1G_{m2}}}, Q_{p2} = \sqrt{\frac{C_4G_{m3}}{C_3G_{m4}}} \quad (11)$$

With the equations (10) and (11), we proceed to design four bandpass filters to filtering the following brain waves: $\delta(1-4Hz)$, $\theta(4-8Hz)$, $\alpha(8-12Hz)$, and $\beta(13-40Hz)$, with central frequency of 2.5, 6, 10 and 26.5 Hz, respectively, and using for these filters the OTAs 3, 1, 2 and 4 for each, respectively.

Then, according to Eq. 9 and 10, we can find capacitors values found for the filters, using the OTAs designed in table 1. We show the filters detail in the table 4.

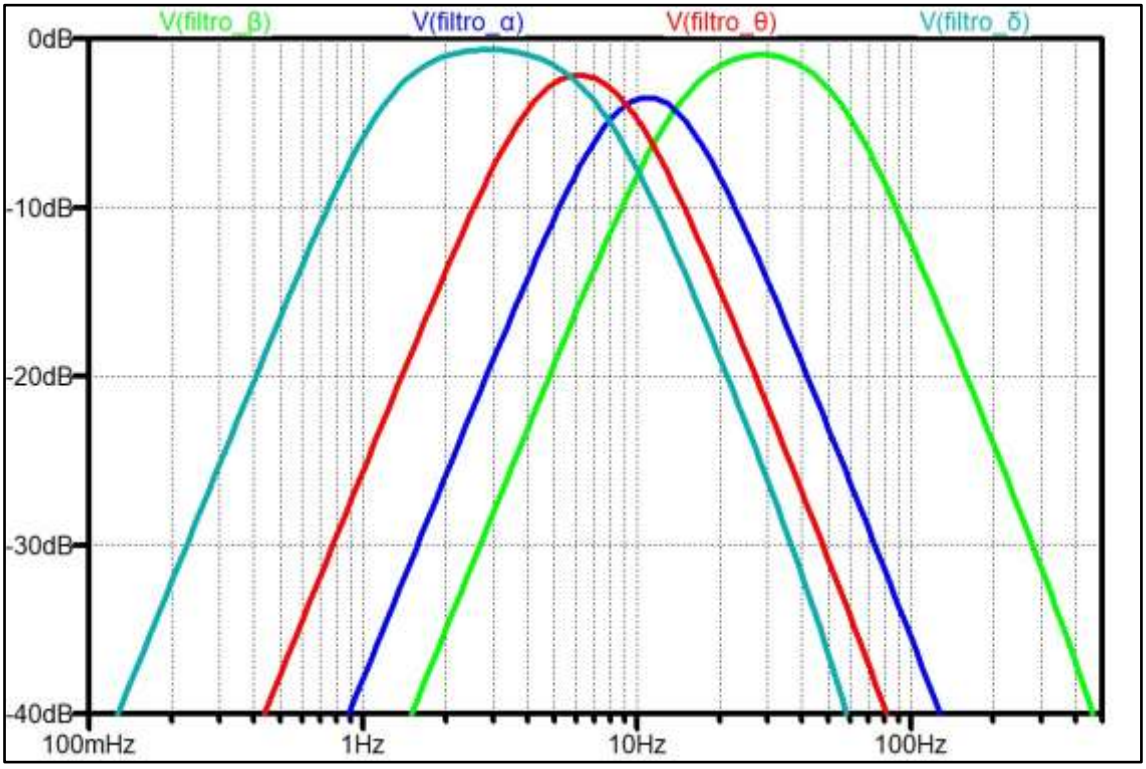
Table 4.
Summary of the Filters Designed with the OTAs

Filter	F_C (Hz)	C_1 (pF)	C_2 (pF)	C_3 (pF)	C_4 (pF)	I_{BIAS} (nA)	Power (uW)	Area (mm^2)
1	2.5	43	19	230	110	480	4.8 uW	0.3
2	6	125	61	250	122	480	4.8 uW	0.18
3	10	164	79	248	120	480	4.8 uW	0.2
4	26.5	73	36	259	120	480	4.8 uW	0.14

In Fig. (9) we show the Bode Diagram of the designed filter above. We can see a good agreement among the theorical estimate and the simulation results.

ISSN (Digital): 2519-5719

Figure 9.
Filters Bode Diagram



5. Conclusions

In this work we can demonstrate that the application of the ACM model with the S-P technique that divided the current and the input transconductance, allow us obtain low output transconductance values and extended input linear range. Further, this work presented the improvement in relation to \cite{campana} in terms of linear range, power consumption and area.

All the OTAs in the table 1, were applied to the low central frequency filter design successfully. The power consumption were in microwatts and they not use a lot area.

For future survey, we attempt place the capacitors on chip. For this target, we can scaling the transconductance/capacitors by 10.

6. References

[1] Veeravalli, Sanchez-Sinencio y S. Martinez, «Different operational transconductance Amplifier topologies for obtaining Very Small Transconductances, » de ISCAS 2000-IEEE International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland, 2000.

[2] R. Campana y M. Marquez, «Diseño de OTAs de Bajo GM y su aplicación en Baja Frecuencia y Microconsumo,» de IBERCHIP, March 14-16, Lima, Peru, 2007.

[3] A. Arnaud y C. Galup-Montoro, «Pico A/V Range CMOS Transconductors Using Series-Parallel Current Division, » Electronics Letters, vol. 39, nº 18, pp. 1295-1296, 2003.

[4] A. Cunha, M. Schneider y C. Galup-Montoro, «An MOS Transistor Model for Analog Circuit Design, » IEEE Journal of Solid-State Circuits, vol. 33, nº 10, pp. 1510-1519, Octuber 1998.

[5] F. Krummenacher y N. Joehl, «A 4-Mhz CMOS continuous time filter with on-chip automatic tuning, » IEEE Journal of Solid-State Circuits, vol. 23, nº 3, p. 750–758, 1988.

[6] A. Arnaud, R. Fiorelli y C. Galup-Montoro, «On the Design of Very Small Transconductance OTAs with Reduced Input Offset,» de SBCCI´05, Florianópolis-Brasil, 2005.

[7] C. Galup-Montoro, M. Schneider y R. Loss, «Series-Parallel Association of FETs for High Gain and High Frequency Applications, » IEEE Journal of Solid-State Circuits, vol. 29, nº 9, pp. 1094-1101, 1994.

[8] G. Düzenli, Y. Kiliç, H. Kuntman y A. Ataman, «On the Design of Low Frequency Filters Using CMOS OTAs Operating in the Subtreshold Region,» Microelectronics Journal, vol. 30, nº 1, pp. 45-54, 1999.

ISSN (Digital): 2519-5719

Trayectoria académica

Franco Renato Campana Valderrama

Universidad Ricardo Palma, Perú.

Ingeniero Electrónico graduado en la Universidad Ricardo Palma (2006). Pasante en la Universidad Católica del Uruguay (2007). Master en el área de Circuitos y Sistemas Integrados por la Universidad Federal de Santa Catarina- Brasil (2010). Graduado del Programa de Entrenamiento en Herramientas CADENCE para Diseño de Circuitos Integrados en Modo Mixto, CT-1, CI-Brasil, Porto Alegre (2011).

Estudiante de Doctorado en la Universidad Federal de Minas Gerais. Ganador del concurso de Subvenciones y Publicaciones de Ciencia e Innovación Tecnológica-CONCYTEC (2011), para la publicación del libro de su autoría “Los Dispositivos Semiconductores”. Áreas de interés: Investigación y desarrollo en el Modelamiento del Transistor MOS, técnicas de Diseño de Amplificadores con Ultra Bajo Consumo de Potencia y Baja Tensión de Alimentación, Diseño de Referencias de Tensión Independientes de la temperatura, y docencia en estas áreas.

Hasta el 2024, docente de la Universidad Ricardo Palma y de la Universidad Peruana de Ciencias Aplicadas.

Autor corresponsal: franco.campana@urp.edu.pe

Orcid: https://orcid.org/0000-0002-1395-8280

Contribución de autoría

Único autor, quien hizo la investigación total del tema del artículo.

Conflicto de intereses

El autor sostiene que no existen conflicto de intereses en el desarrollo de la investigación.

Responsabilidad ética y legal

El desarrollo de la investigación se realizó bajo la conformidad de los principios éticos del conocimiento, respetando la originalidad de la información y su autenticidad. Se han citado las fuentes con sus respectivos datos, y no me ha atribuido algún concepto o filosofía planteada. Todos han sido asignados a sus respectivos autores.

Declaración sobre el uso de LLM (Large Language Model)

Este artículo no ha utilizado para el desarrollo de la investigación textos provenientes de LLM (ChatGPT u otros).

Financiamiento

La presente investigación ha sido financiada con los recursos propios del autor.

Agradecimiento

A los Doctores Alfredo Arnaud Maceira, Joel Gak Szollozy y Matías Miguez de Mori, miembros del Departamento de Ingeniería Eléctrica DIE, de la Universidad Católica del Uruguay.

Correspondencia: franco.campana@urp.edu.pe

ISSN (Digital): 2519-5719