3D STACKED IMAGER AND DIGITAL COUPLING NOISE

Cámara de imágenes apiladas en 3D y ruido de acoplamiento digital

Fernando Raymundo Luyo[1]

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ABSTRACT
High integration circuits like an imager can change its silicon implementation or layout topology using 3D integration technology. Also, this technology can allow the integration of digital circuits at the pixel level. This integration can affect sensible signals of the image sensor and they are not easy to estimate. This study is focus in an approximate method to calculate the impact of adding digital at the pixel in a 3D stacked imager (digital coupling noise). It will take into account all the influences of the stacked wafers. In addition, it will be calculated and compared the coupling between sensible signals in a pixel of a monolithically and a 3D stacked imager. It's found that the digital coupling noise does not affect sensible signals in small array formats, but is not the case in large arrays. This coupling could have the same LSB value of a 10bit ADC, and could add noise to sensible signals.

Keywords: 3D stacked imager; Digital coupling noise; pixel; array; wafer level; ADC; digital pixel.

RESUMEN
Los circuitos de alta integración como un generador de imágenes pueden cambiar su implementación de silicio o la topología de diseño mediante la tecnología de integración 3D. Además, esta tecnología puede permitir la integración de circuitos digitales a nivel de píxeles. Esta integración puede afectar las señales sensibles del sensor de imagen y no son fáciles de estimar. Este estudio se enfoca en un método aproximado para calcular el impacto de agregar digital en el píxel en una cámara de imágenes apiladas en 3D (ruido de acoplamiento digital). Tendrá en cuenta todas las influencias de las obleas apiladas. Además, se calculará y comparará el acoplamiento entre señales sensibles en un píxel de un monolítico y un generador de imágenes apilado en 3D. Se encontró que el ruido de acoplamiento digital no afecta a las señales sensibles en formatos de matriz pequeña, pero no es el caso de matrices grandes. Este acoplamiento podría tener el mismo valor LSB de un ADC de 10 bits y podría agregar ruido a las señales sensibles.

1 INPT-ENSEEIHT, University of Toulouse and Universidad Ricardo Palma.
E-mail: Fernando.Raymundoluyo@alumni.enseeiht.fr

I. INTRODUCTION

The integration of circuits in an imager has facilitated to reduce time processing and to improve external tasks. For example, the integration of an ADC at the pixel level permits not only the conversion of the photonic signal but also to increment the frame rate [1]. Nevertheless, many publications said this kind of implementation will reduce the fill factor in the pixel [2, 3] and have a coupling between the digital to analog part called "digital coupling noise" [1].

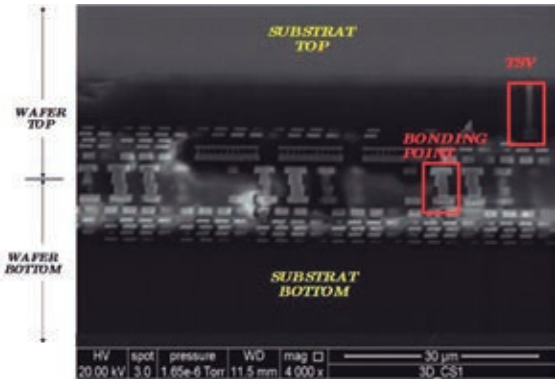

Fig. 1. Cross section of the 3D stacked imager showing the 2 wafers.

In this study, we introduce an approximate method to calculate this noise in both cases: in a monolithically and in a 3D stacked imager. The architecture for this comparison is referred to [4], in which we integrate at the *pixel level*[2] a CDS, 2 source followers, a 10 bits ADC at the top wafer, a 10 bit SRAM at the bottom wafer, and so 101 transistors in total using a 130nm technology node. This technology will be use along of this study. The fig.1 and fig. 2 show the cross section and the pixel view of the 3D stacked imager respectively. The 3D integration technology has allowed us to change the topology of the imager's architecture [4] and this method will permit us to know the impact of this topology variation to the analog signals.

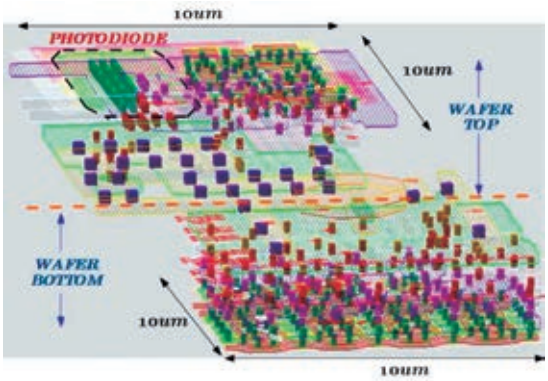

Fig. 2. Pixel view of the 3D stacked imager showing the analog and digital part.

2 The size of the 3D stacked pixel: 10x10um^2.

II. DIGITAL COUPLING NOISE ON IMAGE SENSORS

The publication [1] indicates for first time this kind of coupling in a *digital pixel*. We can interpret this like the coupling between line wires, when a periodic signal is capable to generate a parasitic amplitude which can corrupt another signal. This is more frequently between digital to analog blocks.

A. Coupling on monolithically circuits

To formalize this coupling or crosstalk, we are going to use the same techniques of signal integrity of monolithically circuits [5]. Fig. 3 shows two line wires separated with a defined distance, in which one of them is connected to a digital voltage source. When the voltage source is working in a wire line, it generates an electric field that can reach the other wire, producing a parasitic amplitude or "diaphonic amplitude" in the other line wire through to the parasitic coupling capacitance, C_C. Fig. 4 shows the electrical model of the wires and the coupling capacitance. This model assumes that the system is working at frequencies below of 1.0GHz.

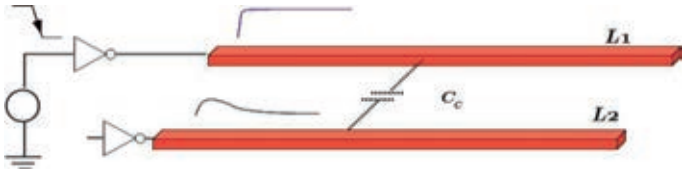

Fig. 3. Digital coupling noise between 2 line wires.

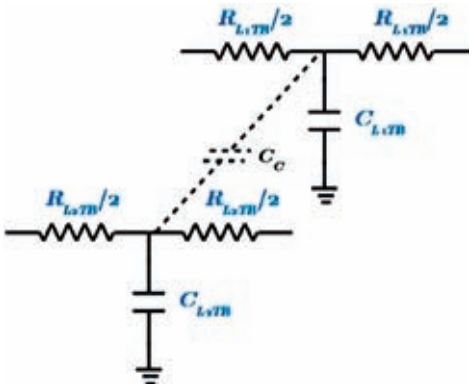

Fig. 4. A "Lump" Electric model of the line wires and the coupling capacitance.

B. Coupling on 3D stacked circuits

As we can see at the fig. 1, the chosen 3D integration technology permits to stack 2 wafers[3]. To proceed the calculation of coupling, we can assume the digital and the analog line wires in different wafers, so a very large separation between them[4] (fig. 5). In addition, we need to know how much influence of one wafer can have to the line wires of the other one.

3 The 3d wafer level integration technology, using a Thermocompression bonding.

4 In a monolithically circuit, this separation is closer due to limitations of the technology.

Different publications [5-7] permit us to calculate this influence in terms of capacitances in monolithically circuits, but they are not adapted to 3D stacked circuits, because they cannot take into account all the wafers and its dimensions. So, we can use numerical methods like RWM to find the influence of wafers [8].

To calculate this in an approximate way, we use the principles of *superposition* and *virtual ground*. First, we calculate the dimensions of the line wires[5]. This information is used to calculate the resistance and capacitance referred to wafers top *T* and bottom *B*. In our case, the line wire's resistor, R_{LiTB}, is calculated using the conventional formulas [9]. To calculate the equivalent capacitance to all wafers, C_{LiTB}, of one of the line wires, we assume it is alone (fig. 6).

The value of this capacitance is done respecting the dimensions of the formula [5]: 0.02 < W/H < 5.12 and 0.02 < T/H <5.12. The equation 1, shows the capacitance C_{LiW} referred to one wafer, including the vertical C_V and fringe C_F capacitances.

$$C_{LiW} = \sum_W (C_V + 2C_F) \qquad (1)$$

This 3D stacked circuit is composed in this example by 2 wafers, so we have the equivalent capacitances referred to the top wafer C_{LiT} and to the bottom wafer, C_{LiB}. They are not referred to the same ground (analog and digital). In practical, we can use the "virtual ground" principle [10] to join them into one reference[6], so we can assume the digital ground as the same as analog ground. This assumption can allow us to work at the middle of the function of probability corners [11]. The final value of this capacitance including the influence of all wafer is C_{LiTB}, it is shown in the following equation. We do the same for the other line wire, C_{L2B}.

$$C_{LiTB} = \sum (C_{iT+} C_{iB}) \qquad (2)$$

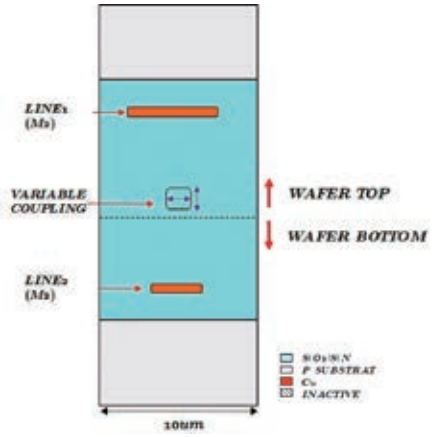

Fig. 5. A 3D stacked circuit of 10um of width. Top and bottom wafers. A variable capacitance for parametric simulation.

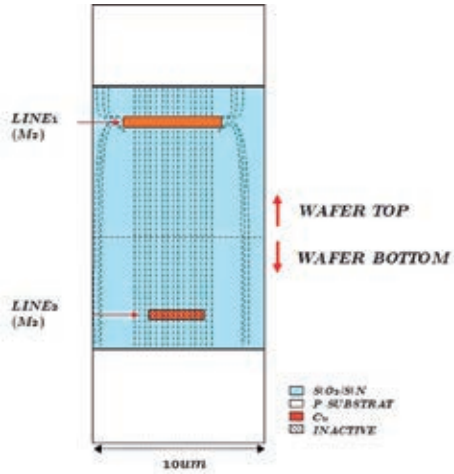

Fig. 6. A 3D stacked structure showing the capacitances in top and a bottom wafer. We use the principle of superposition to calculate the equivalent capacitance referred to the wafers.

To calculate the coupling capacitance, we can use the formulas of [5, 6] taking into account the dimensions and distance² of the line wires.

5 A software was implemented to calculate the dimensions of line wires using image processing from pixel's cross sections.

6 They don't have the same value. But, the mean value of the digital ground is close to zero.

To analyse the impact of this coupling effect in a 3D stacked circuit, we calculate the values of the equivalent capacitances, coupling capacitance and the resistances of the line wires (table 1). Then, we can use the same electric model shown in fig. 4, because the wire lines are referred to the same ground.

Elements at L = 0.2um	**Capacitance [fF]**	**Resistance [Ohms]**
Line wire 1	0.079	1.503
Line wire 2	0.065	0.837

Table 1. Values of the capacitance and resistance of line wires of a 3D stacked circuit.

The result of this simulation is referred in terms of "diaphonic amplitude" to the 3D stacked circuit (fig. 7). To see more details of this effect, we have changed the value of the coupling capacitance in a parametric way (fig. 5). We have used also a 50.0MHz signal to simulated the digital signal. This result, show us that the diaphonic amplitude, DA, is related on 2 aspects: more density of circuits between the studied line wires and different distance separation of them (equation 3).

$$DA = f(\text{Density of circuits, distance}) \qquad (3)$$

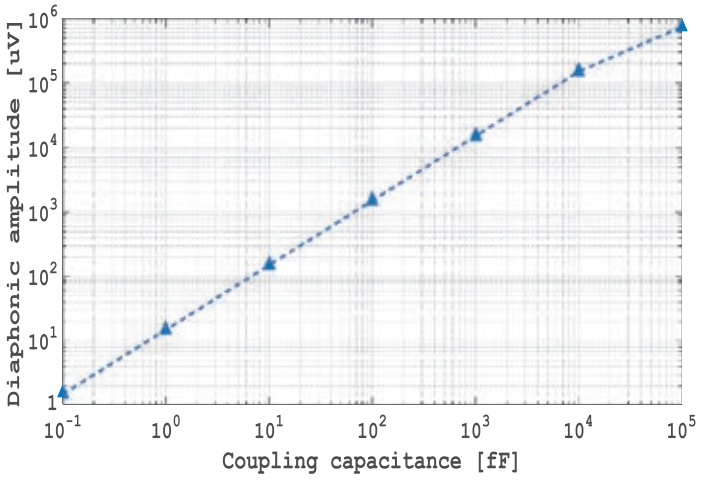

Fig. 7. Diaphonic amplitude in a 3D stacked circuit in function of the capacitive coupling.

C. Digital coupling noise in a 3D stacked imager

In this part, we are going to calculate and compare the effect of the digital coupling noise in a pixel and then into a column line array of pixels. To start this calculation, we have implemented in CADENCE a monolithically pixel with the same circuits of [4]. The figure 8 and 9 shows the digital and analog line wires at the pixel level of the monolithically and 3D stacked imager. We can see that the digital signals are close to the analog one in less of 4um in a monolithically pixel, this will gen-

erate a big coupling capacitance [5, 6]. In the other part, the 3D stacked pixel, separates the digital from the analog line wires in more than 10um.

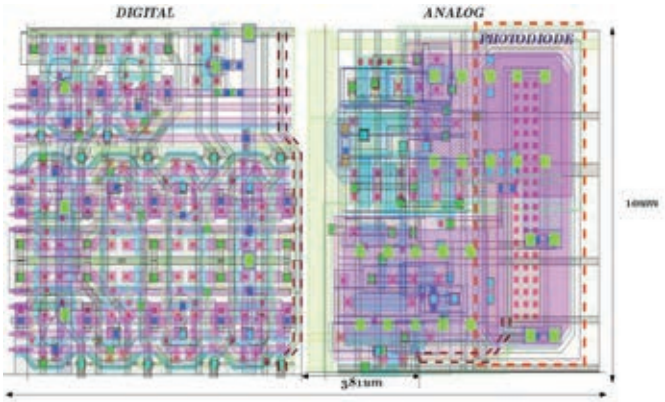

Fig. 8. Pixel LAYOUT view of the monolithically imager showing the analog and digital line wires.

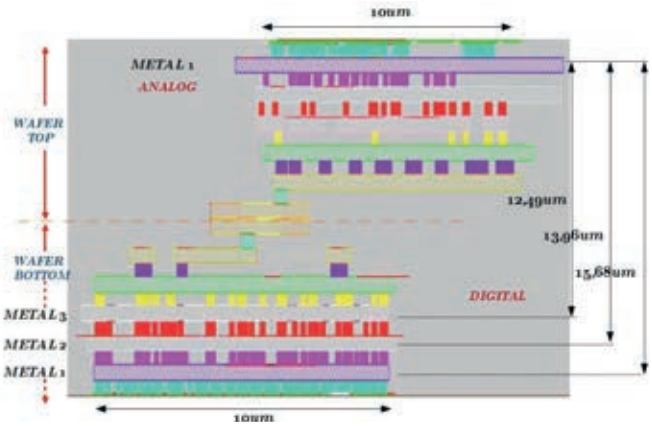

Fig. 9. Pixel LAYOUT view of the 3D stacked imager showing the analog and digital line wires.

Using the dimensions and the separation of line wires (table 2), we have calculated all the passive elements and we put them all to the previous electric model. The result of this coupling in terms of diaphonic amplitude in a pixel is shown in figure 10.

Using a digital power source of 3.3V, a 10bit ADC, and the LSB value is 3.22mV. The value of coupling in a monolithically pixel is less than 10uV. So there is no loss to the analog signal.

Pixel's line wire	T[um]	W[um]	H[um]	S[um]
Digital line, M2	0.42	10	4.002	3.81
Photodiode line wire, M1	0.31	3.15	1.225	3.81

Table 2. Dimensions of the analog and digital wires of a monolithically imager. The analog signal is situated in metal 1. T for thickness; W for width; H pour height and S pour separation.

To calculate this coupling into a 3D structure, we use different digitals lines situates in metal 3, metal 2 and metal at the bottom wafer (fig. 9).

	T[um]	W[um]	H1[um]	H2[um]	S[um]
M3B_M1T	0.42	3.15	4.165	13.475	12.49
M2B_M1T	0.42	3.15	3.15	15.43	13.96
M1B_M1T	0.42	3.15	1.225	16.905	15.68

Table 3. Dimensions of the analog and digital wires of 3D stacked imager. The M3B_M1T means the line wire is situated in the metal 3 level at the bottom wafer and the other line in the metal 1 at the top wafer.

Comparing the LSB value in a pixel in a 3D stacked imager, we can see that the diaphonic amplitudes are less of 2uV. So, they cannot reach a LSB value.

If we increment the number of pixels into 1000 pixels (fig. 10), we can see a direct impact to the analog values into a digital number in a monolithically column line array, they can surpass easily the value of 2 LSB. In the case of the 3D stacked imager, the diaphonic amplitude is still less of 1 LSB even with the digital line wire that is closer to the analog signal (M3B_M1T). This result is due to the change of topology. The digital signals in a 3D stacked imager can be constructed in another wafer, so highly separated. This new topology can reduce the coupling of line wires in more than 70% comparing with a monolithically image sensor.

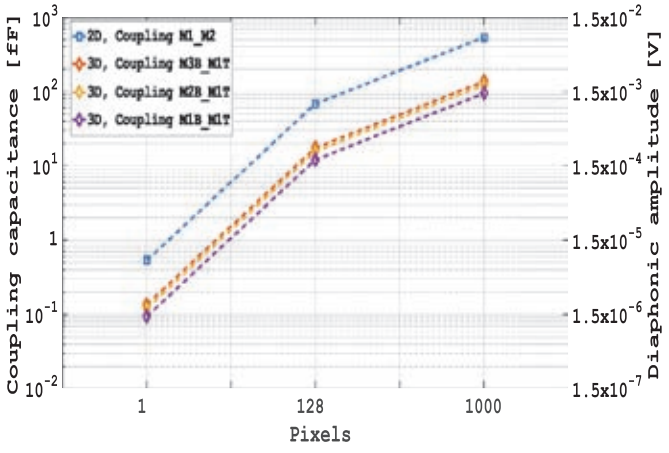

Fig. 10. Simulations for the coupling capacitance and the diaphonic amplitude for a 3D stacked imager. For more than 1000 pixels, we can have a volatge level that can affet the analog signals in a monolithically image sensor.

CONCLUSIONS

The implementation of imagers using a 3D integration technology can allow a change in the topology of pixel's architecture. If we integrate an ADC at the pixel level, it can originate an effect called "digital coupling noise". To calculate this coupling between a digital to analog line wires, we have

employed an approximate method, in where we use the principle of "superposition" and "virtual ground", to take into account the influence of all wafers of a 3D stacked imager. The result of this coupling is the diaphonic amplitude.

The diaphonic amplitude is related to the density of circuits around of the studied line wires and its separation. We have used the previous method to compare this coupling using a digital pixel in a monolithically and 3d stacked imager, using a 10bit ADC. Simulations using a 130nm technology node, show us, that using one pixel, so much for the monolithically and 3D stacked imager, the diaphonic amplitude does not affect the analog value. But, if we put together more pixels (more than 1000), in a monolithically column array, we will have a diaphonic amplitude that can exceed 2 LSB values and affect directly the analog signal. In the other case, putting together more 3D stacked pixels, the diaphonic amplitude still have a diaphonic amplitude less of 1 LSB.

We have seen that stacking circuits permit us to have more than 50% of the value of separation and the reduction in more than 70% of the coupling between sensible line wires compare to a monolithically circuit. Adding circuits at the pixel level can add noise to the sensible signals and its impact must be calculated to know in how much it could affect to the performance of the imager.

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